CONTINUOUS SELF-VERIFY OF CONFIGURATION MEMORY IN PROGRAMMABLE LOGIC DEVICES

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ABSTRACT

A programmable logic device (PLD) such as an FPGA or CPLD is

supplementally configured to verify the integrity of its configuration data during

10   operation of the device. The programmable logic device includes a checksum

calculation engine to calculate a checksum based upon the configuration data. A

checksum comparator compares the calculated checksum to a previously-

calculated checksum to verify the integrity of the configuration data.